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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 02/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,894	ELIAS ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001 and 28 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9-11,16,18,21,23-25,27 and 29* is/are rejected.

7)☒ Claim(s) *2,7,8,12-15,17,19,20,22,26,28 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-30 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 3/30/2001 and Declaration as received on 6/28/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title similar to the following is suggested: Reduction of priority and elimination of instructions whose results are not used by other instructions within an instruction window.

6. The abstract of the disclosure is objected to because it is not written in complete English sentences, but rather in short, non-narrative sentence fragments. Correction is required. See MPEP § 608.01(b).

7. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

8. The disclosure is objected to because of the following informalities: The specification contains no summary section. See below.

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data shet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000. Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the

applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) **Brief Summary of the Invention**: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(k) Sequence Listing. See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Appropriate correction is required.

Claim Objections

9. Claim 14 is objected to because of the following informalities:

a. Regarding claim 14 lines 2-3, the limitation, "the intervening instruction field of the first instruction entry to be set to indicate" is recited. Please change the claim language to read, "the intervening instruction field of the first instruction entry **is to be** set to indicate," so as to make the claim read more correctly.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 3-5, 23-25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Arnold et al., U.S. Patent No. 6,470,445.

12. Regarding claim 1, Arnold has taught a method comprising:

a. Examining a first instruction to determine a first destination that the first instruction will write on (see Col.1 lines 39-53 and Col.8 lines 45-50), the first instruction to be in an instruction window (see Col.3 lines 10-15 and Col.6 lines 19-34, 47-53),

b. Examining a second instruction to determine a first source that the second instruction will use and a second destination that the second instruction will write on (see Col.1 lines 39-53 and Col.8 lines 45-50), the second instruction to enter the instruction window (see Col.3 lines 10-15 and Col.6 lines 19-34, 47-53),

c. Setting a written-on bit associated with the first instruction to a written-on state if the first destination and the second destination will be the same operand (see Col.1 lines 54-62 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

d. Setting a used bit associated with the first instruction to a used state if the first destination and the first source will be the same operand (see Col.1 lines 39-53 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated

that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

e. Determining a priority of the first instruction from the written-on and used bits (see Col.8 lines 45-67). Here, newer instructions are stalled based upon both written-on and used conditions so that an error does not occur, creating a priority favoring the instruction that needs to complete processing before the other instructions can.

13. Regarding claim 3, Arnold has taught the method of claim 1, further comprising:

a. Determining that the first instruction is useless if the first destination and the second destination are the same operand and if no instruction to enter the instruction window after the first instruction and before the second instruction will use the first destination as a source for the at least one instruction to enter the instruction window after the first instruction and before the second instruction (see Col.9 lines 44-58).

14. Regarding claim 4, Arnold has taught the method of claim 3, further comprising eliminating the first instruction from the instruction window (see Col.9 lines 44-58).

15. Regarding claim 5, Arnold has taught the method of claim 4, wherein the eliminating of the first instruction is delayed until the second instruction writes on the second destination (see Col.9 lines 44-58).

16. Regarding claim 23, Arnold has taught a circuit comprising:

a. A written-on logic to determine a written-on bit (see Col.1 lines 54-62 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

b. A used logic to determine a used bit (see Col.1 lines 39-53 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

c. A priority logic to determine a priority based on the written-on and the used bits, the written-on, used and priority logics to be associated with a first instruction entry of a plurality of instruction entries in an instruction window (see Col.8 lines 45-67), the plurality of instruction entries to include a second instruction entry, the first instruction entry to be occupied by a prior instruction and the second instruction entry to be occupied by a subsequent instruction, the first and second instruction each include a source and a destination (see Col.3 lines 10-15 and Col.6 lines 19-34, 47-53). Here, newer instructions are stalled based upon both

written-on and used conditions so that an error does not occur, creating a priority favoring the instruction that needs to complete processing before the other instructions can.

17. Regarding claim 24, Arnold has taught the circuit of claim 23, further comprising the written on logic to set the written on bit to a written on state if the destination of the subsequent instruction is the same operand as the destination of the prior instruction (see Arnold, Col.1 lines 54-62 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Arnold, Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

18. Regarding claim 25, Arnold has taught the circuit of claim 23, further comprising the used logic to set the used bit to a used state if the source of the subsequent instruction is the destination of the prior instruction (see Arnold, Col.1 lines 39-53 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Arnold, Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

19. Regarding claim 27, Arnold has taught the circuit of claim 23, further comprising:

a. An intervening instruction logic to determine whether a third instruction entry of the plurality of instruction entries is occupied by an instruction that intervenes between the prior instruction and the subsequent instruction (see Col.9 lines 44-58).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 6, 9-11, 16, 18, 21 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arnold et al., U.S. Patent No. 6,470,445, in further view of Eisen et al., U.S. Patent No. 6,098,168.

22. Regarding claim 6, Arnold has taught the method of claim 3 as taught above, but has not explicitly taught wherein the method further comprises recording whether the instruction was useless.

23. However, Eisen has taught the recording of an instructions status so that it can be used to further process the instruction and those instructions that depend on it (see Col.4 line 61 – Col.5 line 12). One of ordinary skill in the art would have recognized that it is desirable to record events and information about the execution of instructions so that the information can be used in further processing of the instruction and its dependent instructions. Therefore, one of ordinary

skill in the art would have found it obvious to modify the processor of Arnold to record whether the instruction was useless so that the designation of useless could be used in further processing of the instruction and dependent instructions.

24. Regarding claim 9, Arnold has taught a processor comprising:

a. An instruction window including a plurality of instruction entries including a first instruction entry and a second instruction entry, each instruction entry including an instruction field to be occupied by an instruction (see Col.3 lines 10-15 and Col.6 lines 19-34, 47-53),

b. A fetcher to store a prior instruction in the first instruction entry and to store a subsequent instruction in the second instruction entry, the prior instruction and the subsequent instruction include a source and a destination (see Col.11 lines 29-35).

25. Arnold has not explicitly taught wherein each instruction entry includes a written-on bit, a used bit and a priority field.

26. However, Eisen has taught the computation of a written-on state and its subsequent storing in a field associated with an instruction entry in the dispatch unit so that unnecessary instructions can be eliminated at issue time before data hazards have a chance to occur and cause incorrect results, as well as eliminating hardware from the issue unit (see Col.4 line 61 – Col.5 line12). Because one of ordinary skill in the art would have recognized that it is desirable to eliminate data hazards prior to them becoming hazardous, and that in an out-of-order processor that the issue stage is the first time that it can be determined if the data hazards would be harmful. Therefore, one of ordinary skill in the art would have found it obvious to modify the

processor of Arnold to include a field associated with an instruction in an instruction entry for storing a written-on state so that data hazards can be detected and eliminated at issue time.

27. Furthermore, Arnold has taught the computation of written-on state and used states (see Arnold, Col.8 lines 47-49), as well as a priority signal (see Arnold, Col.8 lines 45-67). Here, newer instructions are stalled based upon both written-on and used conditions so that an error does not occur, creating a priority favoring the instruction that needs to complete processing before the other instructions can. Arnold has taught the computation of these states and the signal in the issue unit (see Arnold, Col.8 lines 21-50). However, Eisen has taught the storing of a written-on state in a field associated with an instruction in an instruction entry so that hazard condition computation can take place in the dispatch unit, but be enforced in the issue unit, thereby eliminating much complex hardware (see Eisen, Col.4 line 61 – Col.5 line 12). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Arnold to store the hazard states which it is already detecting in fields associated with an instruction in an instruction entry so that all of the hazards can be computed in the dispatch unit and enforced in the issue unit, thus saving on hardware space in the issue unit.

28. Regarding claim 10, Arnold in view of Eisen has taught the processor of claim 9, wherein the written-on bit of the first instruction entry to be set to a written-on state if the destination of the prior instruction and the destination of the subsequent instruction are the same operand (see Arnold, Col.1 lines 54-62 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Arnold, Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the

comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

29. Regarding claim 11, Arnold in view of Eisen has taught the processor of claim 9, wherein the used bit of the first instruction entry to be set to a used state if the source of the subsequent instruction and destination of the prior instruction are the same operand (see Arnold, Col.1 lines 39-53 and Col.8 lines 45-50). Here, because write-after-write hazards are detected by conventional methods (see Arnold, Col.8 lines 47-49) consisting of checking the destinations of two instructions for equality, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the result of the comparison only has two possible results, equal or not equal, the signal inherently has a bit value of either zero or one.

30. Regarding claim 16, Arnold in view of Eisen has taught the processor of claim 9 as shown above, but has not explicitly taught where the processor is further comprised of being configured to record a priority of at least one instruction.

31. However, Eisen has taught the recording of an instructions status so that it can be used to further process the instruction and those instructions that depend on it (see Col.4 line 61 – Col.5 line 12). One of ordinary skill in the art would have recognized that it is desirable to record events and information about the execution of instructions so that the information can be used in further processing of the instruction and its dependent instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Arnold to record the priority of an instruction so that the priority could be used in further processing of the instruction and dependent instructions.

32. Regarding claim 18, Arnold has taught a computer system comprising:

a. A processor including:

I. An instruction window having a plurality of instruction entries including a first instruction entry and a second instruction entry, each instruction entry including an instruction field to be occupied by an instruction (see Col.3 lines 10-15 and Col.6 lines 19-34, 47-53),

II. A memory (44 of Fig.1),

III. A fetcher to fetch instructions from the memory and to store a prior instruction in the first instruction entry and to store a subsequent instruction in the second instruction entry, both the prior instruction and subsequent instruction include a source, a destination (see Col.11 lines 29-35), a written on bit of the first instruction entry to be set to a written on state if the destination of the prior instruction and the subsequent instruction are the same operand, and a used bit of the first instruction entry to be set to a written on state if the destination of the prior instruction and the subsequent instruction are the same operand, and the used bit of the first instruction entry to be set to a used state if the source of the subsequent instruction and the destination of the prior instruction are the same operands (see Arnold, Col.1 lines 54-62 and Col.8 lines 45-50). Here, because write-after-write and read-after-write hazards are detected by conventional methods (see Arnold, Col.8 lines 47-49) consisting of an equality check for various sets of operands in the instructions, there is inherently a signal generated that represents the result of the comparison and is associated with each instruction. Because the

result of the comparison only has two possible results, equal or not equal, the signals inherently have a bit value of either zero or one.

33. Arnold has not explicitly taught where each instruction entry includes a written-on bit, a used bit, and a priority field determined from the written-on and used bits.

34. However, Eisen has taught the computation of a written-on state and its subsequent storing in a field associated with an instruction entry in the dispatch unit so that unnecessary instructions can be eliminated at issue time before data hazards have a chance to occur and cause incorrect results, as well as eliminating hardware from the issue unit (see Col.4 line 61 – Col.5 line12). Because one of ordinary skill in the art would have recognized that it is desirable to eliminate data hazards prior to them becoming hazardous, and that in an out-of-order processor that the issue stage is the first time that it can be determined if the data hazards would be harmful. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Arnold to include a field associated with an instruction in an instruction entry for storing a written-on state so that data hazards can be detected and eliminated at issue time.

35. Furthermore, Arnold has taught the computation of written-on state and used states (see Arnold, Col.8 lines 47-49), as well as a priority signal (see Arnold, Col.8 lines 45-67). Here, newer instructions are stalled based upon both written-on and used conditions so that an error does not occur, creating a priority favoring the instruction that needs to complete processing before the other instructions can. Arnold has taught the computation of these states and the signal in the issue unit (see Arnold, Col.8 lines 21-50). However, Eisen has taught the storing of a written-on state in a field associated with an instruction in an instruction entry so that hazard condition computation can take place in the dispatch unit, but be enforced in the issue unit,

thereby eliminating much complex hardware (see Eisen, Col.4 line 61 – Col.5 line 12). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Arnold to store the hazard states which it is already detecting in fields associated with an instruction in an instruction entry so that all of the hazards can be computed in the dispatch unit and enforced in the issue unit, thus saving on hardware space in the issue unit.

36. Regarding claim 21, Arnold in view of Eisen has taught the system of claim 18 as shown above, but has not explicitly taught where the processor is further comprised of being configured to record a priority of at least one instruction.

37. However, Eisen has taught the recording of an instructions status so that it can be used to further process the instruction and those instructions that depend on it (see Col.4 line 61 – Col.5 line 12). One of ordinary skill in the art would have recognized that it is desirable to record events and information about the execution of instructions so that the information can be used in further processing of the instruction and its dependent instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Arnold to record the priority of an instruction so that the priority could be used in further processing of the instruction and dependent instructions.

38. Regarding claim 29, Arnold in view of Eisen has taught the circuit of claim 23 as shown above, but has not explicitly taught where the processor is further comprised of being configured to record a priority of at least one instruction.

39. However, Eisen has taught the recording of an instructions status so that it can be used to further process the instruction and those instructions that depend on it (see Col.4 line 61 – Col.5 line 12). One of ordinary skill in the art would have recognized that it is desirable to record

events and information about the execution of instructions so that the information can be used in further processing of the instruction and its dependent instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Arnold to record the priority of an instruction so that the priority could be used in further processing of the instruction and dependent instructions.

Allowable Subject Matter

40. Claims 2, 7-8, 12-15, 17, 19-20, 22, 26, 28 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record has taught a method for eliminating useless instructions, including determining if there are intervening instructions, but has not taught determining the number of intervening instructions, setting the used bit to a default value based on the type of instruction, or the prediction of an instruction as useless, as well as predicting its priority, based upon the history of the instruction. These further limitations are not taught in the prior art of record, or any combination of the prior art of record, and thus would be allowable if rewritten in independent form as described above.

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the

references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

42. Lotz, U.S. Patent No. 5,805,851, has taught a method of determining WAW and RAW hazards between instructions within a bundle and storing the dependency information.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
2/4/2004

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